

REMARKS

Claims 1-12, 21-24 and 28-38 are all of the claims presently pending in the application. Claim 38 has been merely editorially amended.

Entry of this Amendment is believed proper since no new issues are being presented to the Examiner that would require further consideration and/or search.

Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-12, 21-24 and 28-38 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Joshi et al. (U.S. Patent No. 6,921,982; hereinafter “Joshi”).

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention of exemplary claim 1 is directed to a double-gate field effect transistor.

The transistor includes a strained-silicon channel formed adjacent a source and a drain, a first gate formed over a first side of the channel, a second gate formed over a second side of the channel, a first gate dielectric formed between the first gate and the strained-silicon channel and a second gate dielectric formed between the second gate and the strained-silicon channel (e.g., see Application at page 3, lines 8-14).

II. THE PRIOR ART REFERENCE

The Examiner alleges that Joshi teaches the claimed invention of claims 1-12, 21-24 and 28-38. Applicant submits, however, that there are elements of the claimed invention

which are neither taught nor suggested by Joshi.

That is, Joshi does not teach or suggest “*a double-gate field effect transistor*”, as recited in claim 1, and similarly recited in claims 21, 30 and 31.

Applicant maintains the traversal arguments included in the Amendment filed under 37 C.F.R. §1.111 on October 11, 2006, the substance of which is incorporated herein and is not repeated, for brevity.

In the claimed invention, as detailed, exemplarily and schematically, in the B1-B2 cross sectional illustration provided in the Amendment dated October 11, 2006, the gate conductor was “polished” down so that two separated gates (1, 2) are formed. This “polish” of the gate conductor was taught by Joshi as the method to obtain the device of Fig. 8F from the device shown by Fig. 8C (col. 10 lines 5-9).

Channel 32, as shown in the A1-A2 cross-sectional illustration of Figure 8F of Joshi provided in the Amendment dated October 11, 2006) of Joshi forms an inverted U shape that warps over a core 24. The vertical portions of the outer surface of channel 32 are covered with a gate oxide 33 and are gated by gate 88 and gate 89, respectively. The inner surface of channel 32 is not gated since it is in contact with a core 24. Core 24 is not a gate, nor is there a gate oxide present between core 24 and the inner surface of channel 32.

The channel 8 (Si Fin) (e.g., see the B1-B2 cross sectional illustration provided in the Amendment dated October 11, 2006) has two vertical surfaces. Each of these surfaces is covered with a gate oxide and is gated by gate 1 and gate 2, respectively. The carriers in the channel are therefore controlled effectively by gate 1 and gate 2. This is not the case for the carriers in channel 32 of Joshi, where the two gates are distanced by the core 24. Even if core 24 were made ultra thin, there is no gate oxide that coats the inner surface of channel 32. As a result, only one surface of the channel 32 is gated as the other (inner) surface is in contact with

the core 24 and is not gated.

The above discussion explains why Joshi's structure is not a Fin-FET nor a double-gate transistor in spite of his use of the term "Fin-FET" to describe the structure.

Furthermore, with respect to exemplary dependent claim 38, Joshi does not teach or suggest "*wherein said first channel comprises a first vertical surface covered by said first gate dielectric and a second vertical surface covered by said second gate dielectric*".

Indeed, as pointed out above, channel 32 of Joshi forms an inverted U shape that warps over a core 24. The vertical portions of the outer surface of channel 32 are covered with a gate oxide 33 and are gated by gate 88 and gate 89, respectively. The inner surface of channel 32 is not gated since it is in contact with a core 24. Core 24 is not a gate, nor is there a gate oxide present between core 24 and the inner surface of channel 32.

Furthermore, with respect to exemplary dependent claim 37, Applicant submits that Joshi does not teach or suggest "*wherein carriers in said channel are controlled by said first gate and said second gate*".

The Examiner erroneously alleges that Joshi "discloses that carriers in the channel are inherently controlled by the first gate and the second gate" (see Office Action dated January 17, 2007 at page 5).

Applicant submits that the Examiner has clearly failed to meet his burden for establishing that the feature recited in exemplary dependent claim 37 inherent.

Applicant points out that "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." (See M.P.E.P. § 2112 IV; emphasis in M.P.E.P. itself). Indeed, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized

by persons of ordinary skill’.” (See M.P.E.P. § 2112 IV; emphasis added by Applicant).

Furthermore, “[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.” (See M.P.E.P. § 2112 IV; emphasis added by Applicant).

Applicant points out that the Examiner has not provided any basis in fact and/or technical reasoning or extrinsic evidence to support his vague allegation of inherency. Indeed, the Examiner’s allegation appears to be nothing more than the Examiner’s personal opinion.

Moreover, the Examiner alleges that “ ‘when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent’.” (See Office Action dated January 17, 2007 at page 5). The Examiner, however, has not considered Applicant’s arguments provided in the Amendment dated October 11, 2006.

Applicant again points out that the carriers in the channel cannot be controlled effectively in Joshi, because the two gates are distanced by the core 24. Even if core 24 were made ultra thin, there is no gate oxide that coats the inner surface of channel 32. As a result, only one surface of the channel 32 is gated as the other (inner) surface is in contact with the core 24 and is not gated.

Applicant points out that the Examiner must answer all material traversed by the Applicant. Specifically, “[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of applicant’s argument and answer the substance of it.” (See M.P.E.P. § 707.07(f)).

Applicant points out that several lengthy and specific traversal arguments were included in the amendment filed on October 11, 2006. The Examiner, however, has repeated

the same prior art rejection and merely provided general comments in response to Applicant's arguments. If the Examiner wishes to maintain this rejection, Applicant respectfully requests the Examiner to specifically respond to each of Applicant's specific arguments.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggest by Joshi. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 1-12, 21-24 and 28-38, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

Serial No. 10/645,646

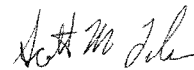
13

Docket No. YOR920030328US1

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: March 19, 2007



Scott M. Tulino, Esq.
Registration No. 48,317

Sean M. McGinn, Esq.
Registration No. 34,386

**MCGINN INTELLECTUAL PROPERTY
LAW GROUP, PLLC**

8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 48150